Before conducting the experiment, it is important to cover some analytical calculations that will be essential to understanding if the experiment is going smoothly. The first thing to do is calculate the range of duty cycles where the circuit operates at DCM and the range that it operates at CCM. To do this we can use the formula of Vo/Vi for DCM and equate it with Vo/Vi in CCM which is the duty cycle. This gives:

$$\left(\frac{V_O}{V_I}\right)_{CCM} = \delta = \left(\frac{V_O}{V_I}\right)_{DCM} = \frac{1}{1 + \frac{2fLI_O}{V_I\delta^2}}$$

Because the output current is fixed, it is feasible to find the range of duty cycles where the circuit operates at DCM. Specifically, for $V_I = 5V$, pwm frequency $f = 62.5kHz$, $I_O = 0.06A$ and $L = 100\mu H$

We can solve the quadratic equation which has roots: $\delta = 0.19$ and $\delta = 0.82$. Between these values, the BUCK SMPS is in DCM and outside the roots it is operating in CCM.

With a fixed current, changing loads between measurements has the effect of changing the duty cycle of the PWM wave. Essentially, changing load has the effect of changing V_o as :

$$V_O = R_{load} * I_O = R_{load} * 0.06$$

This equation does not take into account any parasitic resistance of the inductor of the Buck and it is stated to explain the linear relationship between the load and the output voltage in our experiment. Depending on if the circuit is in CCM or DCM, the Arduino code will regulate the duty cycle so that the output current is 0.06A. Having the boundary values of the duty cycle for CCM and DCM and using the relationship between the load and the output voltage we can easily find the resistance values that give us these boundary duty cycles:

For $\delta = 0.19$:

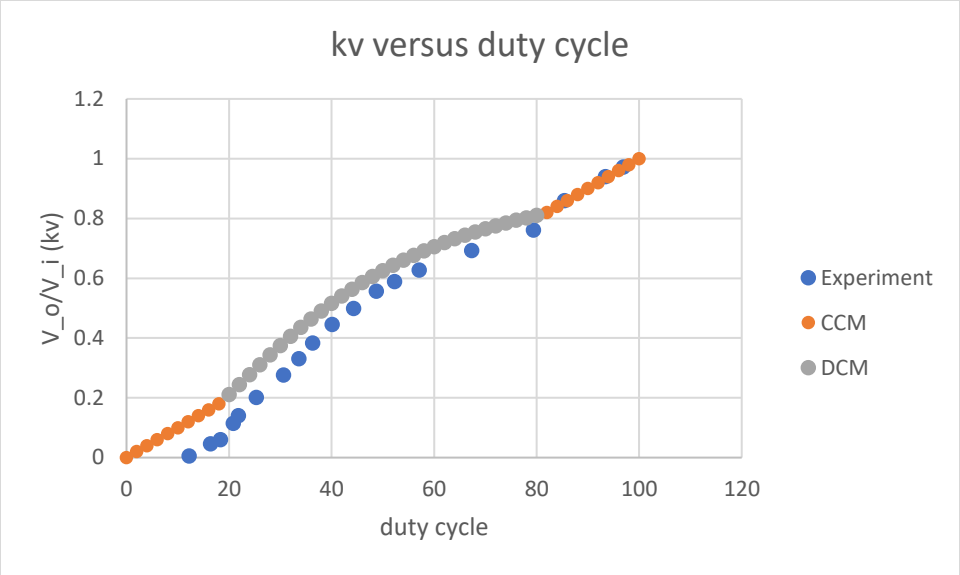
$$R_{load} = \frac{V_O}{I_O} = \frac{V_O}{I_O} * \frac{V_I}{V_I} = \delta * \frac{V_I}{I_O} = 0.19 * \frac{5}{0.06} = 15.8\Omega$$

For $\delta = 0.82$:

$$R_{load} = \delta * \frac{V_I}{I_O} = 0.82 * \frac{5}{0.06} = 68.3\Omega$$

To proceed with the experiment we need to take adequate measurements with loads between these 2 values to examine DCM operation and adequate measurements outside of this range to examine CCM.

Having a high-level expectation of what to expect allows to continue with taking measurements for various loads:



Having done the experiment and comparing with theory, one can draw some really interesting conclusions regarding the circuit's operation and why it behaves like that. The most important thing to note, is that there is a clear discrepancy between the measured data and the theoretical results for small values of the duty cycle. A somewhat odd observation is that the measured duty cycle for an almost 0 value of kv is 12% (implying dissipation of energy). This clearly is different than what is expected considering the theory and it can only be attributed to one factor: power losses. Specifically, an intuitive explanation would be that the duty cycle deviates from theory because energy that is supplied by the input source (which is regulated by the duty cycle of the PWM wave) is dissipated in inefficient components of the circuit and is not stored in the capacitor of the SMPS which raises the output voltage, so firstly enough energy must be supplied to cover the inefficiencies and then the output voltage starts rising. The important next step is identifying that component that leads to such inefficiencies. To help draw that conclusion, one should focus on the fact that as duty cycle rises, the deviation between theory and experiment is becoming smaller and smaller and thus to find what is causing the problem, one should find why increasing the duty cycle makes the efficiency of the system better. The duty cycle has the role of determining the amount of time that the capacitor is charging (which is when the PWM wave is high) and when the capacitor is discharging (when the PWM wave is low). Having low duty cycle means that the capacitor is mostly discharging, and the component that allows this discharging path is a diode(because it is non-synchronous buck). The conclusion is that the diode has high voltage drops that are not taken into account from the theory and its great power dissipation leads to high discrepancies in the graph. Increasing the duty cycle, decreases the use of the diode which makes the efficiency of the system better which also implies that any power dissipation on the switching transistor is negligible compared to the diode. Other than that, the shape of the kv curves is as expected and the ranges of CCM and DCM are almost identical to the ones calculated from theory. To reduce such inefficiencies a synchronous buck circuit could be used that uses an extra transistor on the discharging path that leads to lower power dissipation.